Intersil's Radiation Hardened Low Power FPGA Power Solutions

Introduction

Due to its flexibility in design, FPGA based systems have become increasingly common in space applications. One of the most commonly used IC's in the space industry are the radiation tolerant low power FPGA's. This application note discusses the ISL_LOWPWRMEZ_EV1ZA board, Intersil's reference power design for low power radiation hardened FPGA's. This particular board is optimized to power an Actel RTAX FPGA and features the ISL70003SEH and ISL75051SEH as the POL regulators for the core, auxiliary, and I/O voltages needed in the FPGA.

FPGA Power Solution

The core voltage for the RTAX is 1.5V and is regulated by the ISL70003SEH directly from the 12V intermediate bus. A secondary ISL70003SEH is used to create a 5V rail, which will be in the inputs to the LDO's. This is done to reduce the overall system noise. Two ISL75051SEH IC's regulate the necessary 1.8V and 3.3V for the auxiliary and I/O supplies, respectively (see Figure 1).

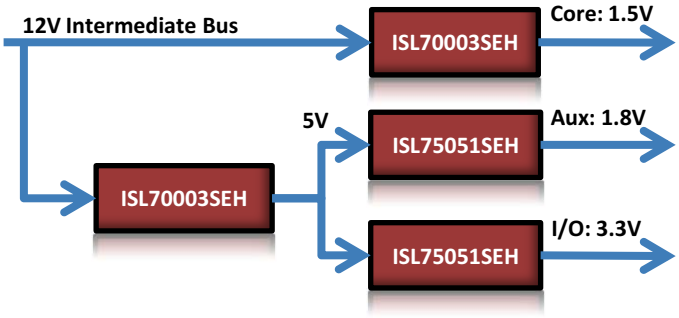

FIGURE 1. BLOCK DIAGRAM OF POWER DISTRIBUTION

The ISL70003SEH is a radiation hardened and SEE hardened high efficiency, monolithic synchronous buck regulator with integrated MOSFETs. This single chip power solution operates over an input voltage range of 3V to 13.2V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. The ISL70003SEH uses voltage mode architecture with feed-forward and switches at a fixed frequency of 500kHz or 300kHz. Loop compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance. The ISL70003SEH can provide up to 3A of continuous output current at a T_J = +150°C and 6A at T_J = +125°C.

The ISL75051SEH is a radiation hardened, low voltage, high current, single output LDO specified for up to 3A of continuous output current. It can operate over an input voltage range of 2.2V to 6V and is capable of providing output voltages of 0.8V to 5V with an external resistor divider. Typical dropout voltages seen with the ISL75051SEH are 65mV at 1A load current and 225mV at 3A.

Circuit Description

An AC/DC adapter provides the input source through the 2.1mm barrel-jack connector. Once the board is enabled, both ISL70003SEH parts start up at the same time. To ensure proper sequence during power-up is maintained, the PGOOD line of both ISL70003SEH's are OR'ed together and connected to the ENABLE pin of the ISL75051SEH's. This ensures that the core voltage is up first, followed by simultaneous start up of the auxiliary and I/O voltage once both the core voltage and 5V are at their proper levels.

The output capacitors for each device have been chosen to minimize ESR in an effort to maintain output ripple <1% of the regulated voltage and to optimize the stability of the systems. KEMET's T530 series of tantalum capacitors offer ultra low ESR <15mΩ and are DLA certified.

Provisions for stability measurements are included by replacing R_4, R_{19}, R_{38} and R_{45} with 10Ω to 100Ω resistors and injecting the AC signal across the test points on either side of those resistors.

Radiation Tolerance

Total Ionizing Dose

These circuits are fabricated on a 0.6µm BiCMOS junction isolated process optimized for power management applications. They were hardened by design to achieve a Total Ionizing Dose (TID) rating of at least 100krads(Si) at the standard 50 to 300rad(Si)/s high dose rate as well as the standard <10mrad(Si)/s low dose rate. Well known TID hardening methods were employed such as closed geometry NMOS devices to reduce leakage and optimized bias levels for bipolar devices to compensate for gain reduction. These products are wafer-by-wafer acceptance tested to 50krad(Si) at the standard low dose rate of <10mrad(Si)/s.

Single Event Effects

Both IC's are also hardened by design for Single Event Effects (SEE) to a Linear Energy Transfer (LET) of 86.4MeV • cm^2/mg by employing various SEE hardening techniques such as proper device sizing, filtering and special layout constraints. The ISL75051SEH and the ISL70003SEH exhibit no single event latch-up or burnout up to their respective input voltage at an LET of 86.4MeV • cm^2/mg.

These circuits also offer class leading Single Event Transient (SET) performance. The ISL70003SEH is designed to offer a single LX pulse deviation due to an SET at an LET of 86.4MeV • cm^2/mg. The ISL75051SEH also guarantees a <5% output voltage deviation without the need of additional external filtering. This is important as modern processors and FPGAs can only tolerate a 5% window for the supply voltage and in many cases, the 5% tolerance includes DC voltage tolerance and transients due to load step or release and transients due to SETs.

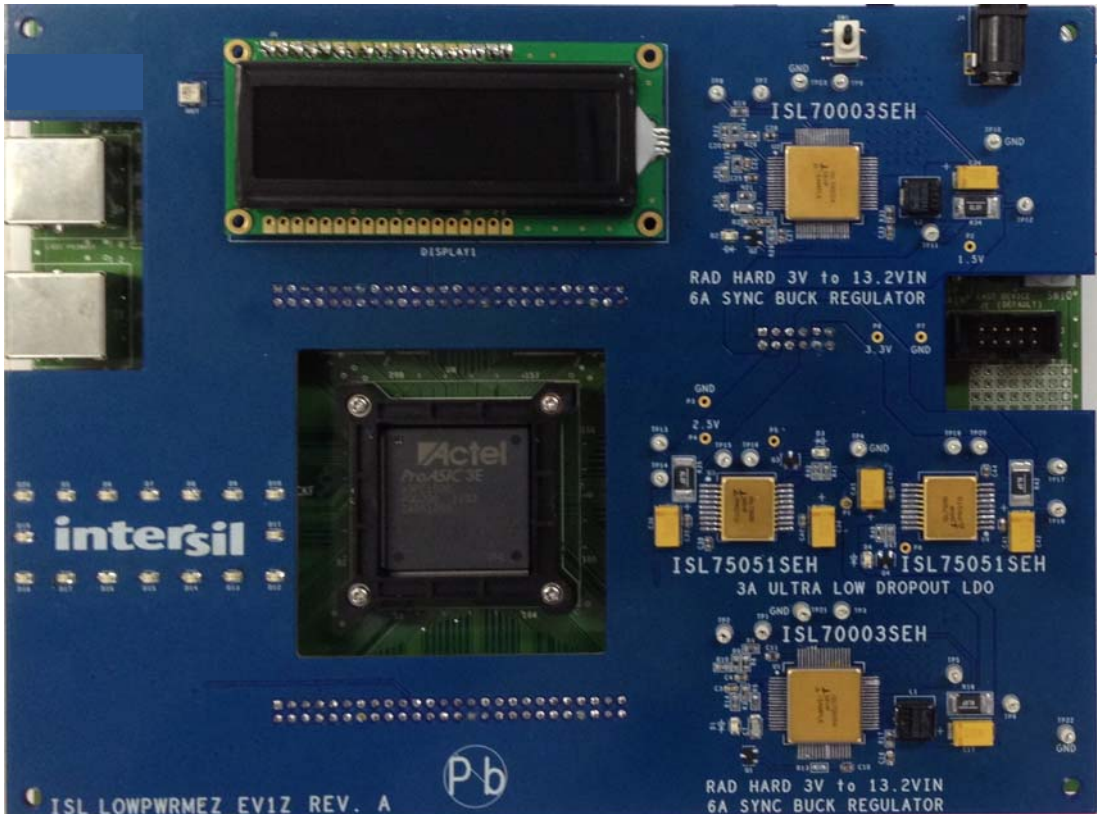

FIGURE 2. LOW POWER RADIATION HARDENED FPGA POWER SOLUTIONS REFERENCE DESIGN

For further information on radiation performance and a complete listing of Applications, Related Documentation and Related Parts scan this QR code with your smart phone or visit us at www.intersil.com/space.